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APPLICATION FOR U.S. LETTERS PATENT

Title:

A Digital Phase Locked Loop

In filing this non-provisional application, I claim the benefit of the filing date of Provisional Application Number 60/421,857 which I filed on 29 October 2002 and which bears the same title (under 35 U.S.C. § 119(e))

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Ar a of the invention

This invention deals with digital synthesis of waveforms, and in particular with the generation of such signal in phase and frequency synchronization with a reference signal, utilizing phase locked loops.

Background of the invention

The phase locked loop (PLL) is a closed loop electronic servo whose output lock onto and tracks an input reference signal. Phase lock is obtained the phase of the output signal with that of a reference, and any phase difference is converted into an error correcting voltage. This error voltage changes the output signal phase to make it track the input.

The servo system is comprised of three basic partitions; a phase detector, a loop filter, and a voltage (or current) controlled oscillator (VCO), as shown in figure 2.

When the phase difference between the VCO output and the reference is constant, the loop is locked. If either the reference input or the VCO output changes phase, the phase detector and the loop filter produce a DC error voltage, proportional in magnitude and polarity to the signal phase change. This error voltage changes the phase of the VCO by altering its frequency, until it lock on the reference input.

To understand the operation of a closed loop servo system refer to figure 1. The following relationships characterize the closed servo loop: and

$$\theta_e(s) = \frac{1}{1+G(s)H(s)} + \theta_r(s)$$

$$\theta_o(s) = \frac{G(s)}{1+G(s)H(s)} + \theta_r(s)$$

, wherein $\theta_r(s)$ is the input phase, $\theta_o(s)$ is the output phase, $\theta_e(s)$ is the phase error, $G(s)$ is the feedforward transfer function, and $H(s)$ is the feedback transfer function.

There are various types and orders for PLLs. The order of a PLL refers to the degree of the polynomial expression $1+G(s)H(s)=0$, which is termed the characteristic equation of the loop. The roots of the characteristic equation become the poles of the closed loop overall transfer function. The type of the PLL refers to the number of poles in the loop transfer function, which are located at the origin of the S-plane. Type 1 PLLs typically utilize a flip-flop, or a sample and hold device to detect the phase error between the reference and the output, while type 2 PLLs typically use a phase / frequency detector to generate the phase error voltage.

Type 2 PLL has two pure integrators $\left(1/s^2\right)$. This approach is utilized when a coherency to a received signal is required, as this type of loop maintains a steady state zero phase error for all operating conditions.

The basic type 2 PLL take the form shown in figure 4. The phase detector is designed to detect phase errors of either polarity relative to the reference signal and produce the properly polarized commands necessary to correct the VCO. The lowpass filter must include an integrator for storing the proper VCO control voltage during phase lock. The basic transfer characteristics for each individual function in the loop are:
K_p the phase detector gain constant in volts per radian;

K_f the filter transfer function

$$K_f = \frac{1 + R_2 CS}{R_1 CS} = \frac{1 + T_1 S}{T_2 S}$$

K_o the VCO sensitivity in radians / sec / volts.

The output to input ratio for this loop is

$$\frac{\theta_o(s)}{\theta_1(s)} = \frac{K_p K_f K_o}{S + K_p K_f K_o} = \frac{1 + T_1 S}{\frac{S^2 T_2}{K_p K_o} + 1 + T_1 S}$$

The loop bandwidth, or natural frequency is

$$\omega_n = \sqrt{\frac{K_p K_o}{T_2}}$$

And the damping factor is

$$\zeta = \sqrt{\frac{K_p K_o}{T_2}} \left(\frac{T_1}{2} \right)$$

Since K_p, and K_o are typically fixed, the parameters T_1, and T_2 are the variables used to control the loop characteristics. These parameters are derived as:

$$T_2 = \frac{K_p K_o}{\omega_n^2} \quad T_1 = \frac{2\zeta}{\omega_n}$$

And the components of the filter are:

$$R_1 = \frac{K_p K_o}{\omega_n^2 C} \quad R_2 = \frac{2}{\omega_n C}$$

This invention describes a phase locked loop wherein a numerically controlled oscillator is used instead of a VCO, counters and digital integrators replace the loop filter and its components, and in a specific case a direct phase digitizer and a subtractor replace the traditional phase detector.

An embodiment of a digital phase locked loop is shown in figure 7. This PLL comprises a modified phase detector, a digital loop filter and a numerically controlled oscillator.

A numerically controlled oscillator (NCO) is a circuit wherein the output signal phase and frequency are directly controlled by digital numerical data inputs. The basic NCO shown in figure 5, is comprised of an adder, a register, a sine lookup (cosine) table, and a digital to analog converter. The numerical input is the desired phase difference $\Delta\Theta$ over a period of one clock cycle T_c. On every clock cycle, the adder adds $\Delta\Theta+\Theta(k)$, wherein $\Theta(k)$ is the accumulated phase on clock cycle k. The number of bits in the adder and the register is n. Whenever the accumulated phase $\Theta(k)$ reaches 2^n the accumulation rolls over and starts accumulating from zero. As the process of accumulation continues, the rollover is repeated, wherein the rate of repetition is defined by the numerical input. The larger the number at the input, the more frequently will the accumulator rollover. As the output of the accumulator is the accumulated phase $\Theta(k)$, each rollover indicates the end one cycle, and the beginning of a new cycle of the output signal.

Typically it is desirable for the oscillator to have an analog sinusoidal output. A sine lookup table, followed by a digital to analog converter is typically used to convert the accumulated phase $\Theta(k)$ into an analog (voltage or current) output.

The coefficient for the NCO can be determined as follows: The numerical input to the NCO is m, and the clock frequency of the NCO is F_c, and the actual angular output frequency is

$$\omega_o = 2\Pi F_c \frac{m}{2^M}$$ wherein M is the number of bits in the NCO's adder. Therefore, $$K_o = 2\Pi \frac{F_c}{2^M}.$$

The phase detector is a device that detects the phase difference (error) between the reference signal and the output signal, and generates an output signal of a magnitude proportional to the size of the error, and in a polarity, which will cause the VCO to correct for the error.

In the digital realm the desired presentation of the error is a numerical quantity. An embodiment of a phase detector capable of generating a numerical output as a measure of the error is shown in figure 6. This is a modified version of the standard phase detector wherein an EXOR gate and a counter are added to provide the numerical output. The output of the EXOR (4) controls the counter such that when the line is "high" the counter counts up, and when the line is "low", the counter resets to zero. If the time (phase error) between the reference and the output is δt, and the frequency of the clock to the counter is F_c, then the output of the counter is $N=\delta t \times F_c$. The coefficient K_p of the detector can be calculated by determining the phase difference

$$\theta = 2\Pi \frac{\delta t}{T_0}$$

Wherein T_0 is the period of the reference input signal. The value N is therefore

$$N = \frac{\theta T_0}{2\Pi} F_c$$

And

$$K_p = \frac{T_0 F_c}{2\Pi}.$$

The properties of the components of the loop filter can be determined from the desired dynamic properties of the loop, ω_n, and ζ. As $T_2 = \frac{K_p K_o}{\omega_n^2}$, and $T_1 = \frac{2\zeta}{\omega_n}$.

Viewing the loop filter as an active filter with an amplifier as shown in figure 4, its response is given by $V_a = V_p \frac{R_2}{R1} + V_p \frac{t}{R_1 C} + V_c(0)$ for $0<t<T_0$, wherein V_p is the voltage output of the phase detector from t=0 to $t=T_0$ (the input signal period), and $V_c(0)$ is the voltage on the capacitor at time 0. For $R_1 = \frac{K_p K_o}{\omega_n^2 C}$ and $R_2 = \frac{2}{\omega_n C}$ then $\frac{R_2}{R_1} = \frac{2\omega_n}{K_p K_o} = \alpha$.

Since the loop is digital, the amplifier response can be viewed as an accumulator (20) followed by an adder (23)as shown in figure 8. The accumulator (20) replaces the integrator t / R_1C, and the adder (23) adds a constant of R_2 / R_1 to the output of the accumulator. In this implementation the accumulator accumulates the value of N on each accumulator clock (24), which is at a rate of T_0 / T_2. The clock to the accumulator (20) is derived from the clock period T_c. If $T_c=\beta T_0$, wherein T_0 is the period of the input reference, then for the accumulator the clock (24) period is $T_a=T_c / \beta T_2$. For simplicity, T_2 may be selected such that βT_2 is a power of 2, to enable easy scaling of the accumulator clock period.

The adder that follows the accumulator adds a constant αN. For simplicity ω_n can be selected such that α is a power of 2, and thus the scaling of N is obtained by shifting the bits.

Another embodiment for a digital phase lock loop is shown in figure 9. The PLL in this embodiment is comprised of a digital phase sampler, a subtractor, a digital filter, and a numerically controlled oscillator.

The digital phase digitizer (40) samples the input signal (49) on every clock transition, and reports the instantaneous phase of the input signal at the time of the clock transition. The NCO (43) used in this embodiment is modified to output phase information instead of the typical analog voltage amplitude, as shown in figure 10. A subtractor subtracts the instantaneous phase generated by the phase digitizer (44), from the instantaneous phase of the NCO (45). The output (46) of the subtractor (41), is the phase error, in terms of phase, and the coefficient of this kind of phase discrimination is therefore K_p=1. The loop filter is similar to the one discussed earlier, and is used to control the dynamic properties of the loop.

Other embodiments of the digital phase locked loop are shown in figures 11, and 12.. These embodiments describe type 1 phase locked loops, and utilize a digital UP / DOWN counter as the loop integrator.

Description of the drawings

Figure 1, shows a basic servo loop diagram.

Figure 2, shows a basic phase locked loop.

Figure 3, shows a type 1 PLL.

Figure 4, shows a type 2 PLL.

Figure 5, shows an embodiment of a numerically controlled oscillator (NCO).

Figure 6, shows an embodiment of a modified phase detector.

Figure 7, shows a block diagram of a digital phase locked loop (PLL).

Figure 8, shows a block diagram of a digital filter for a digital PLL.

Figure 9, shows a block diagram of a different embodiment of a digital PLL.

Figure 10, shows an embodiment of a modified NCO.

Figure 11, shows a block diagram of a type 1 digital PLL.

Figure 12, shows a block diagram of an alternative type 1 digital PLL.

Figure 13, shows an embodiment of a digital loop filter for a digital PLL.

Figure 14, shows an embodiment of a phase digitizer.

Figure 15, shows an embodiment of the phase quantizer section of the phase digitizer.

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To describe the invention, one embodiment is best understood referring to figures 6, 7, 10, and 13. Figure 7, shows an embodiment of a digital phase locked loop, comprised of a modified phase detector, a digital loop filter, and a modified numerically controlled oscillator.

An embodiment of the modified phase detector is shown in figure 6. In steady state conditions, both flip-flops (1, and 2) are set (Q outputs are "1"), and the output (4) of the EXOR gate (8) is low. Under these conditions the gate (5, and 6) are enabled and the counter (3) is reset to "0". On a transition from "1" to "0" on either of the inputs, a flip-flop associated with that input is reset, causing the output (4) of the EXOR gate (8) to change to "1", enabling the counter (3) to count UP, at the rate of its clock. Upon the transition from "1" to "0" on the other input to the detector, the other flip-flop is reset. This causes the output (4) of the EXOR gate (8) to change to "0", resetting the counter (3), and output of the NOR gate (7) changes to "1", setting both flip-flops to their steady state condition. Once the flip-flops are set, the output of the NOR gate (7) changes back to "0", and the detector is ready for the next input transitions. The numerical output of the counter is indicative of the phase error between the inputs to the detector, and is transferred to the digital loop filter just before the counter is reset.

The embodiment of the digital filter is presented in figure 13. In the filter an accumulator (99) is sued to accumulate the phase error input (60), on every transition of its clock. The clock rate to the accumulator is scaled by a scaling factor (69) using the clock scaler (68), and then gated by the gate (67). To prevent the accumulator from rolling over when the accumulation reaches 2^n, Or when it goes down to zero, a limit detector (66) is employed. The limit detector (66) monitors the data in the accumulator, to verify that it is between an upper limit and a lower limit (56). If the data goes above the upper limit, or goes below the lower limit, the limit detector causes the gate (67) to block the clock to the accumulator, and prevent it from rolling over. The output of the accumulator is transferred to an adder (65) where it is added to the output of the error scaler (98). The scaler receives the phase error input (60), and scales it by a the error scaling factor (97). The phase error input (60) may be a positive or a negative number, and the accumulator (62) and the adder (65) have to add the error (60) or subtract it, depending of the most significant bit (64) of the error signal (60). The output (58) of the register (59) is the size of change required from the NCO, which follows the filter. The required change may be positive or negative, and the most significant bit (57) of the output data (58) indicates the polarity of the required change.

Figure 10, shows an embodiment of a modified NCO. The basic NCO is comprised of an accumulator followed by a phase to amplitude converter. In the embodiment shown in figure 10, the accumulator is comprised of the adder (34) and the register (36). The phase to amplitude converter is comprised of the sine lookup table (37) followed by a digital to analog converter.

Typically in NCOs, the input "A" (38) to the adder (34) determines the output frequency of the NCO. In the embodiment of the NCO, presented in figure 10, the input (38), is preceded by an adder (33). On the adder (33), the input "B" receives the phase increment per clock period (32) for the center frequency of the PLL, while on the input "A", the requested change in frequency (31), as determined by the phase detector and the loop filter, is added, or subtracted, to control the NCO in order to lock the loop.

In a different embodiment of a digital PLL shown in figure 9, a phase digitizer (40) and a subtractor (41) replace the phase detector (10) shown in figure 7. Also, the feedback (45) is the digital presentation of the instantaneous phase of the NCO, instead of the feedback (15) derived from the analog output, as is the case shown in figure 7.

An embodiment of the phase digitizer is shown in figure 14, and an embodiment of its quantizer section is shown in figure 15. In the digitizer, the input signal is amplified by the amplifier (70), limited by the hard limiter (71), filtered by the lowpass filter (72), to produce a harmonic free sinewave, and then split into by the quadrature signal splitter (73) into two sinewaves, I (75), and Q (75), which are phased 90° from each other. In the phase quantizer (76) the two quadrature inputs (74, and 75) are used to generate n phase shifted sinewaves, wherein the phase difference between any two adjacent sinewaves is 360 / n. The quantizer (76) applies these sinewaves to n comparators each combined with a flip-flop. On every clock transition the flip-flops output a pattern unique to the to the phase of the sinewaves (74, 75) at the moment of the clock transition. An encoder (77) follows the quantizer and converts the pattern generated by the quantizer (76) into a Binary code (78).

Referring to figure 9, the phase digitizer (40) is followed by a subtractor (41). The subtractor calculates the phase difference between the phase (44) of the reference input signal (49), and the phase (45) of the NCO. The digital filter (42) the follows the subtractor (41), and the NCO (43) that follows the digital filter are similar to the digital filter (11) and the NCO (12) presented in figure 7.